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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,086	10/16/2003	Vishnu K. Agarwal	MICRON.095C1	9081

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EXAMINER	
HU, SHOUXIANG	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 04/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,086	AGARWAL ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *11-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 23-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/16/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 11-22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper dated 12/20/2004.

Claim Objections

Claims 23-33 are objected to because of the following informalities and/or defects:

Claim 23 recites two mutually contradictory subject matters that fluorine diffuses into the dielectric layer and that fluorine diffusion is inhibited.

In addition, the terms of "forming" and "annealing" in claim 23 should read as: --the formation of-- and --an annealing of the--, respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 and 23-33, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being obvious over Lu (Lu et al. EP 854505 A2, of record) in view of Lur (Lur et al., 5,364,803, of record).

Lu discloses a gate structure in an integrated circuit structure (Fig. 3; also see page 4, lines 36-37), comprising: a TiN_xB_y barrier layer overlying a dielectric layer (5; a gate oxide) and underlying a conductive layer comprising tungsten in a gate electrode (14).

Lu further discloses that the gate electrode (14) can be a poly-tungsten stack for lowering the sheet resistance of the gate electrode structure (see page 4, lines 30-31). It is noted that the term of "poly-tungsten stack" commonly means a polysilicon-tungsten stack with a polysilicon layer underlying a tungsten or tungsten silicide layer (as evidenced in Lur et al., 5,364,803; see the polysilicon layer 14 and the tungsten silicide layer 18 in Figs. 1 and 2). And, Lu further discloses that the TiN_xB_y layer can be between the gate stack and the gate dielectric layer (see page 4, lines 35-37).

Although Lu does not expressly disclose that the tungsten-comprised conductive layer in the gate stack can further comprise at least some fluorine atoms, one of ordinary skill in the art would readily recognize that a tungsten or tungsten silicide layer formed in a poly-tungsten gate stack with desired quality and process condition normally inherently comprises at least some fluorine atoms when being formed with the art-known common CVD method that involves a fluorine-containing gas (as evidenced in Lur, see col. 2, lines 28-29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the CVD method of Lur into the making of the device of Lu, so that a gate structure with desired quality would be obtained with desired process condition. And, the TiN_xB_y layer in the above collectively taught device would be naturally capable of functioning as a diffusion barrier layer that prevents the fluorine atoms in the conductive layer from reaching to the underlying dielectric layer.

Regarding claims 2-4, 7, 25-27 and 30, it is noted that the thicknesses of the dielectric layer, the polysilicon layer, the TiN_xB_y layer and the tungsten-containing layer in the gate structure are all art-recognized parameters of importance subject to routine experimentation and optimization. It would be well within the ordinary skill in the art to form these layers in the gate structure with their thicknesses being respectively about 30 to 200 angstroms, about 300 to 1,500 angstroms, about 50-500 angstroms, and about 200 to 4,000 angstroms, through routine experimentation and optimization, as they are all well within or overlapping with the commonly recognized individual ranges for these layers, as further evidenced in Lur (see col. 2, lines 43-64).

Regarding claims 9 and 32, it is noted that it is art-known that an intrinsically doped monocrystalline silicon wafer is a common type of wafer used for forming a semiconductor substrate.

Regarding claims 10 and 33, it is noted that the device in Lu is a memory device that naturally further comprises an operable portion of a transistor array on the substrate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
March 17, 2005

SHOUXIANG HU
PRIMARY EXAMINER